

## Standalone Tag Reader Circuit

### STARC

The Standalone Tag Reader Circuit (STARC) is an integrated circuit dedicated to the automotive immobilizer applications. It combines on the same chip all the circuitry to interface with a transponder : antenna drivers and demodulator.

A low dropout voltage regulator and a physical interface fully compatible with the ISO 9141 norm are also available.

The Standalone Tag Reader Circuit is fabricated with the SMARTMOS™3.5 technology. This process is a double layer metal, 1.4µm, 45V technology, combining CMOS and bipolar devices.

- **Contactless 125kHz tag reader module :**
  - **Self synchronous sample & hold demodulator**
  - Amplitude or phase modulation detection
  - High sensitivity
  - Fast "read after write" demodulator settling time
  - Low resistance and high current antenna drivers : 2Ω @ 150mA (typ.)
  - Bidirectionnal data transmission
  - Multi tag, multi scheme operation.
- **Low dropout voltage regulator :**
  - Wide input supply voltage range : from 5.5V up to 40V
  - Output current capability up to 150mA DC with an external power transistor
  - 5V output voltage with a ± 5% accuracy
  - Low voltage reset function
  - Low current consumption in standby mode : 300µA (typ.).
- **ISO 9141 transmitter and receiver module :**
  - Input voltage thresholds ratiometric to the supply voltage
  - Current limitation
  - Output slew rate control
  - No external protection device required.

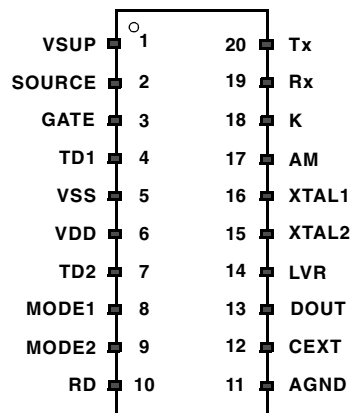
## MC33690

### STANDALONE TAG READER CIRCUIT



**DW SUFFIX**  
Plastic Package  
CASE 751D  
SO - 20

#### Pin Connections



#### ORDERING INFORMATION

Device	Operating Junction Temperature Range	Package
MC33690DW	T <sub>J</sub> = -40°C to 125°C	SOIC 20

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REV 4.8

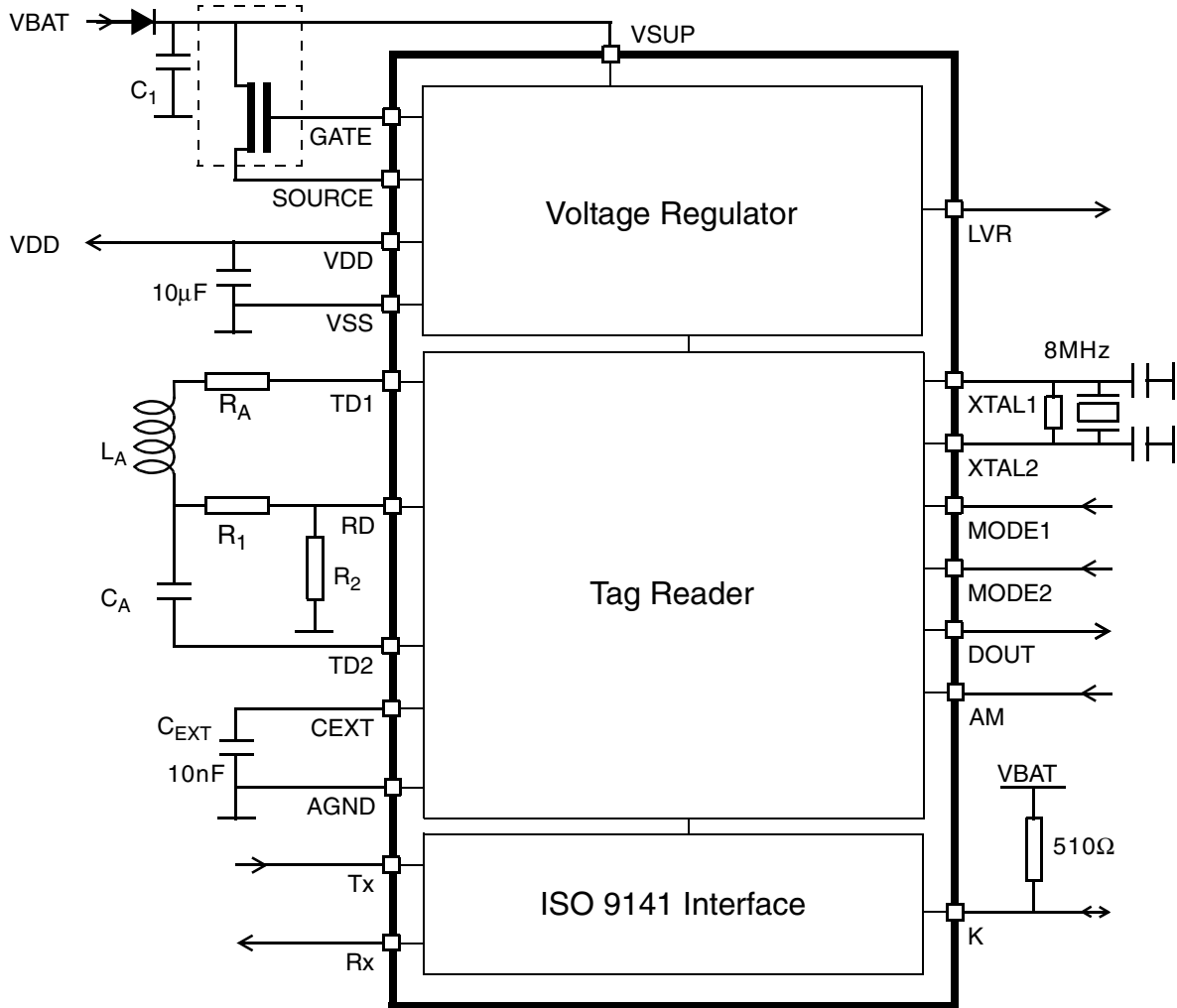
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## BLOCK DIAGRAM

Figure 1 : Standalone Tag Reader Circuit

Optional : external N channel MOS required for sourced current > 50mA.  
A recommended reference is MMFT 3055VL from Motorola.



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## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	$V_{SUP}$	$V_{SS}-0.3$ to +40	V
Supply voltage without using the voltage regulator ( $V_{SUP} = V_{DD}$ )	$V_{DD}$	$V_{SS}-0.3$ to +7	V
Voltage on SOURCE		$V_{SS}-0.3$ to +40	V
Current into/from GATE		0	mA
Voltage on GATE		$V_{SS}-0.3$	V
Voltage on pins : MODE1/2, CEXT, DOUT, LVR, XTAL1/2, Rx, Tx		$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Voltage on RD		$\pm 10$	V
Voltage on K and AM		$V_{SS}-3$ to 40	V
Current on TD1 & TD2 (Drivers on & off)		$\pm 300$	mA
Voltage on AGND		$V_{SS}\pm 0.3$	V
ESD voltage capability (HBM, see note 1)		$\pm 2000$	V
ESD voltage capability (MM, see note 1)		$\pm 200$	V
Solder heat resistance test (10s)		260	$^{\circ}\text{C}$
Junction temperature	$T_J$	170	$^{\circ}\text{C}$
Storage temperature	$T_s$	-65 to +150	$^{\circ}\text{C}$

Note 1 :

Human Body model, AEC-Q100-002 Rev. C.  
Machine Model, AEC-Q100-003 Rev. E.

## THERMAL CHARACTERISTIC

Characteristic	Symbol	Value	Unit
Junction to ambient thermal resistance (SOIC20)	$R_{th}$	80	$^{\circ}\text{C}/\text{W}$

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## PIN FUNCTION DESCRIPTION

Pin	Function	Description
1	VSUP	Power supply
2	SOURCE	External N channel transistor source
3	GATE	External N channel transistor gate
4	TD1	Antenna driver 1 output
5	VSS	Power and digital ground
6	VDD	Voltage regulator output
7	TD2	Antenna driver 2 output
8	MODE1	Mode selection input 1
9	MODE2	Mode selection input 2
10	RD	Demodulator input
11	AGND	Demodulator ground
12	CEXT	Comparator reference input
13	DOUT	Demodulator output (5V)
14	LVR	Low Voltage Reset input/output
15	XTAL2	Oscillator output
16	XTAL1	Oscillator input
17	AM	Amplitude modulation input
18	K	ISO 9141 transmitter output and receiver input
19	Rx	ISO 9141 receiver monitor output
20	Tx	ISO 9141 transmitter input

DESCRIPTION

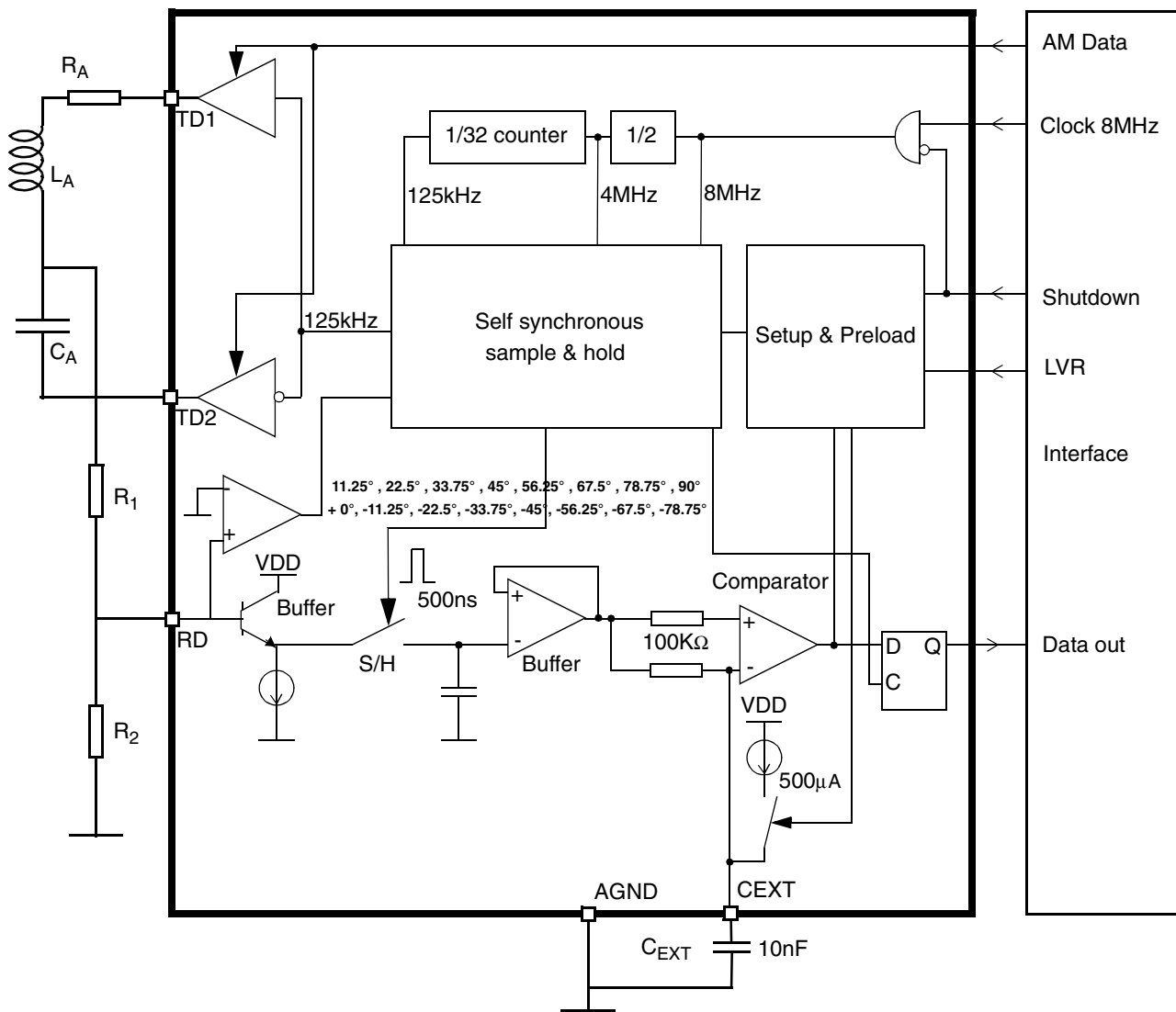
TAG READER MODULE

The Tag Reader module is dedicated for automotive or industrial applications where information has to be transmitted contactless. The tag reader module is a write/read (challenge/response) controller for applications which demand high security level.

The tag reader module is connected to a serial tuned LC circuit which generates a magnetic field power supplying the tag.

The use of a synchronous sample & hold technique allows communication with all available tags using admittance switching producing absorption of the RF field. Load amplitude or phase shift modulation can be detected at high bit rates up to 8kHz. 125kHz is the typical operational carrier frequency of the tag reader module with a 8MHz clock.

Figure 2 : Tag Reader block diagram



## Read function

When answering to the base station, a transponder generates an absorption modulation of the magnetic field. It results in an amplitude/phase modulation of the current across the antenna. This information is picked up at the antenna tap point between the coil and the capacitor. An external resistive ladder down scales this voltage to a level compatible with the demodulator input voltage range (see parameter  $V_{INRD}$  page 16).

The demodulator (see figure 2) consists of :

- an input stage (emitter follower),
- a sample & hold circuit,
- a voltage follower,
- a low offset voltage comparator.

The sampling time is automatically set to take into account a phase shift due to the tolerances of the antenna components (L and C) and of the oscillator. The allowed phase shift measured at the input RD ranges from  $-45^\circ$  to  $+45^\circ$ . Assuming that the phase reference is the falling edge of the driving signal TD1, this leads to a sampling time phase ranging from  $-78.75^\circ$  to  $90^\circ$  with discrete steps of  $11.25^\circ$ . After reset condition, the sampling time phase is  $+11.25^\circ$ .

**The antenna phase shift evaluation is only done :**

- after each wake-up command (see pages 10 to 12),
- or after reset (see page 7).

This is necessary to obtain the best demodulator performances.

In order to ensure a fast demodulator settling time after wake up, reset or a write sequence, the external capacitor  $C_{EXT}$  is preloaded at its working voltage.

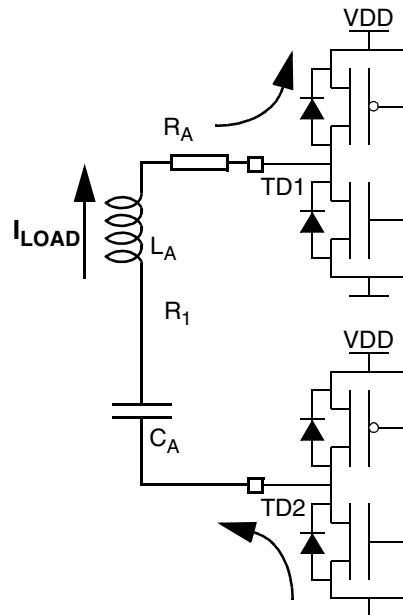
This preset occurs  $256\mu s$  after switching the antenna drivers on and its duration is  $128\mu s$ . After wake up or reset, the preset has the same duration but begins  $518\mu s$  after clock settling. After power on reset,  $VSUP$  must meet the minimum specified value, enabling the nominal operation of VDD, before the start of the preset. Otherwise the preset must be done by the user through a standby/wake-up sequence.

## Write function

Whatever the selected configuration (see page 9), the write function is achieved by switching on/off the output drivers TD1/2.

Once the drivers have been set in high impedance, the load current flows alternatively

**Figure 3 : Current flow when the buffers are switched off**



**VOLTAGE REGULATOR**

The low dropout voltage regulator provides a regulated 5V supply for the internal circuitry. It can also supply external peripherals or sensors. The input supply voltage ranges from 5.5V to over 40V.

This voltage regulator uses a series combination of high voltage LDMOS and low voltage PMOS transistors to provide regulation. An external low ESR capacitor is required for the regulator stability.

The maximum average current is limited by the power dissipation capability of the SO 20 package.

This limitation can be overcome by connecting an external N channel MOS in parallel with the

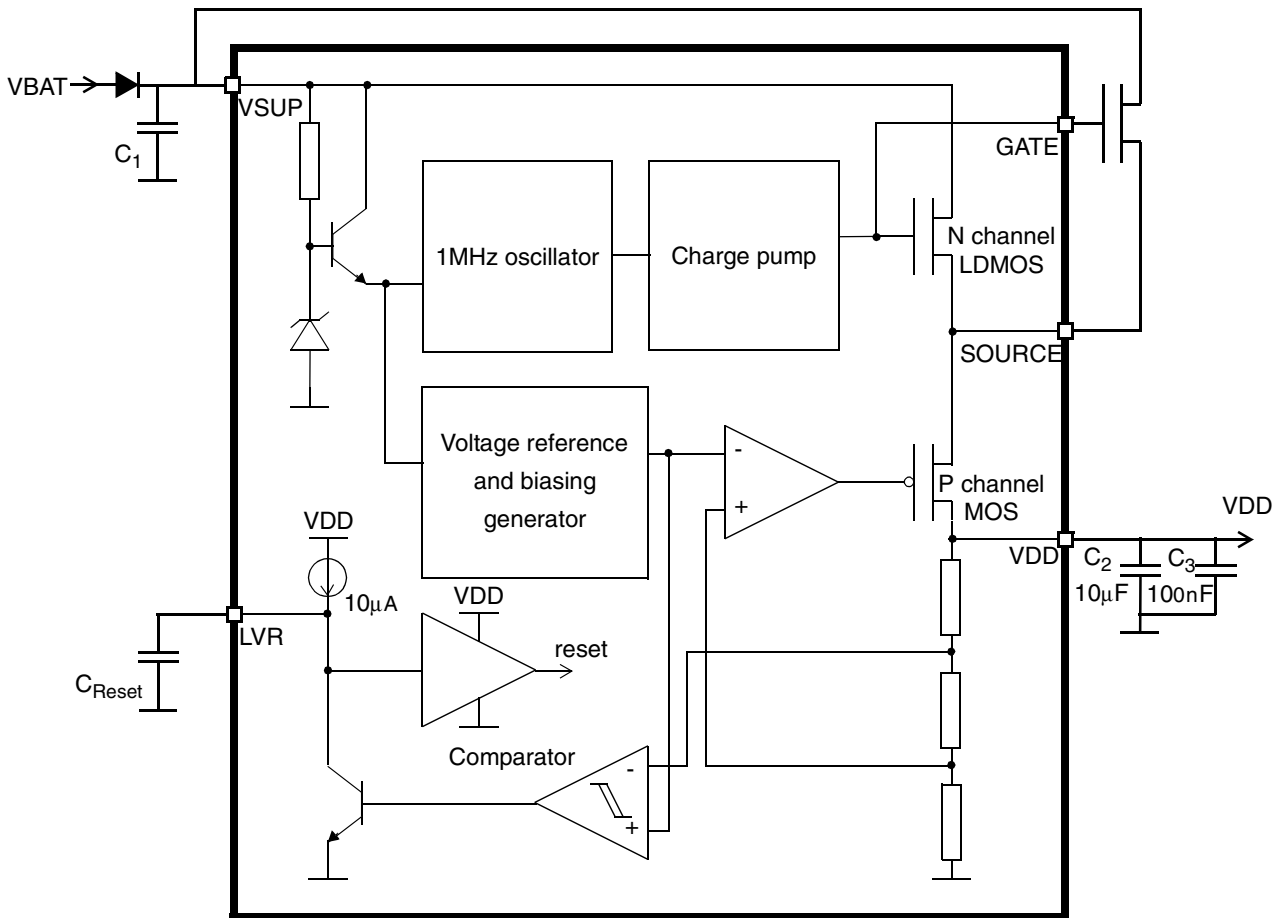
internal LDMOS. The threshold voltage of this transistor must be lower than the one of the internal LDMOS (1.95V typ.) in order to prevent the current from flowing into the LDMOS. Its breakdown voltage must be higher than the maximum supply voltage.

A low voltage reset function monitors the VDD output. An internal 10µA pull-up current source allows, when an external capacitor is connected between LVR and GND, to generate delays at power up (5ms typ. with  $C_{Reset}=22nF$ ).

The LVR pin is also the input generating the internal reset signal. Applying a logic low level on this pin resets the circuit :

- all the internal flip flops are reset,
- the drivers TD1/2 are switched on.

**Figure 4 : Voltage regulator block diagram**



**ISO 9141 PHYSICAL INTERFACE**

This interface module is fully compatible with the ISO 9141 norm describing the diagnosis line. It includes one transmitter (pin K) and 2 receivers (pins K and AM).

The input stages consist of high voltage CMOS triggers. The thresholds are ratiometric to VSUP. A ground referenced current source (2.5µA typ.) pulls down the input when unconnected.

When a negative voltage is applied on the K or AM lines, the input current is internally limited by a 2kΩ resistor (typ.) in series with a diode.

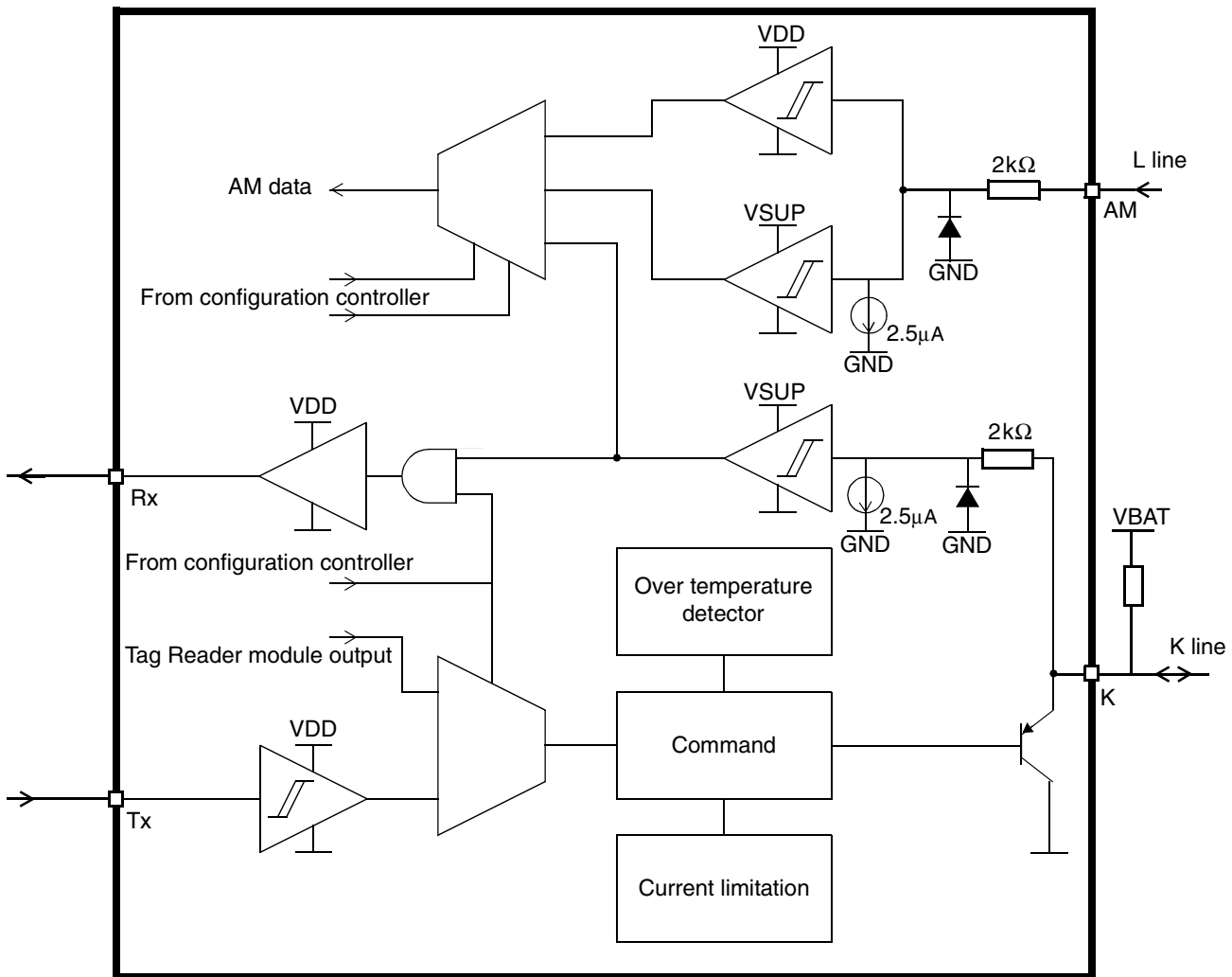
A current limitation allows the transmitter to drive

any capacitive load and protects against short circuit to the battery voltage. An overtemperature protection shuts the driver down when the junction temperature exceeds 150°C (typ). Once shut down by the overtemperature protection, the driver can be switched on again :

- if the junction temperature has decreased below the threshold,
- and by applying an off/on command, coming either from the demodulator in configurations A and B or directly applied on the input Tx in configuration C (see pin K status in table 1 page 9).

The electromagnetic emission is reduced thanks to the voltage slew rate control (5V/µs typ.).

**Figure 5 : ISO 9141interface**





## COMMUNICATION MODES DESCRIPTION

The STARC offers 3 different communication modes. Therefore it can be used as a standalone circuit connected to an Electronic Control Unit

(ECU) through a bus line or it can be directly connected to a microcontroller in case of a single board architecture.

**Table 1. Communication modes description**

Configuration			Configuration pins		Pin status & function description
Type	Bus type	Name	Mode1	Mode2	
Standalone	1 wire (VBAT)	A	0	0	<b>K</b> output/input : - demodulator output, - amplitude modulation input - shutdown/wake-up <b>AM</b> must be connected to VSUP <b>DOUT</b> forces a low level
	2 wires (VBAT)	B	0	1	<b>K</b> output : - demodulator output <b>AM</b> input : - amplitude modulation input, - shutdown/wake-up <b>DOUT</b> forces a low level
Direct connection to a MCU	2 wires (VDD)	C	1	x	<b>DOUT</b> output : - demodulator output <b>AM</b> input : - amplitude modulation input <b>MODE2</b> input : - shutdown/wake-up
				1	<b>K</b> output/input (standalone ISO 9141 interface) : - driven by <b>Tx</b> and monitored by <b>Rx</b>
				0	<b>K</b> input (standalone ISO 9141 interface) : - monitored by <b>Rx</b> - <b>Tx</b> disabled

**STANDALONE CONFIGURATION WITH ONE WIRE BUS**

When a low level is applied on pins MODE1 and MODE2, the circuit is in **configuration A** (standalone single wire bus configuration, see figure 13 page 18).

After power on, the circuit is set into **read mode**. The demodulator output is directly routed to the ISO 9141 interface output K.

The circuit can be set into **write mode** at anytime by violation of all possible patterns on the single wire bus during more than 1ms. Then the K line achieves the amplitude modulation by switching on/off both antenna drivers.

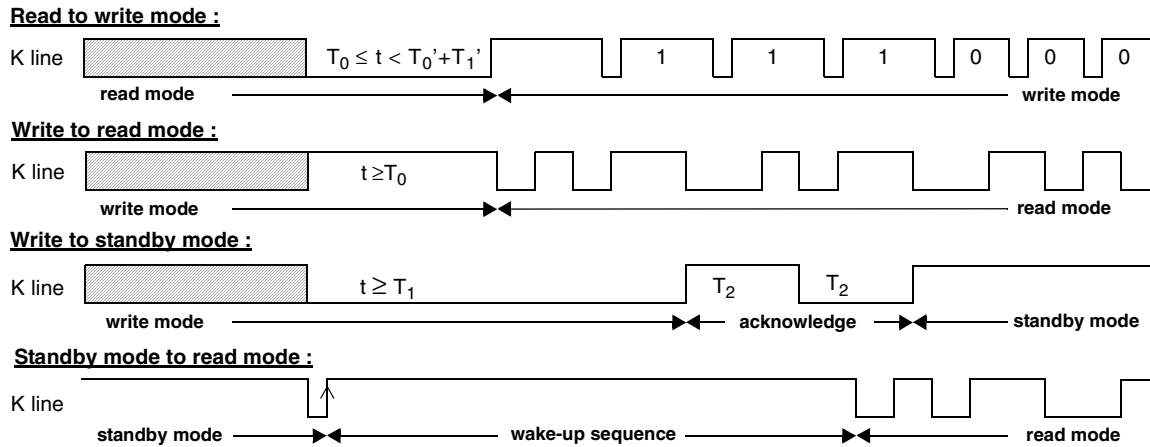
After 1ms of inactivity at the end of the challenge phase (bus in idle recessive one state), the circuit is set back into read mode.

The circuit can be put into **standby mode** by forcing the K line at zero during more than 2 ms after entering the write mode. Once the K line is released, the circuit sends an acknowledge pulse before entering into standby mode.

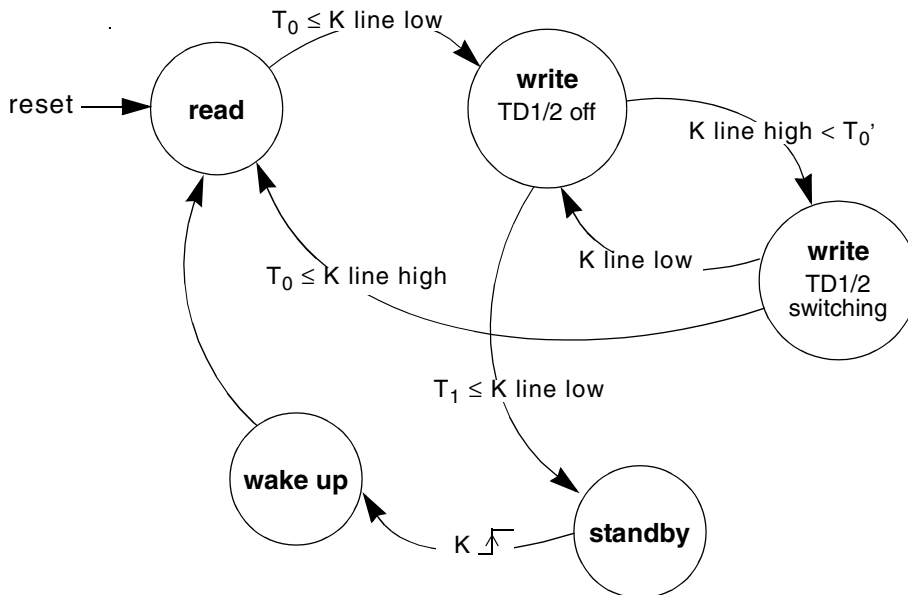
In standby mode, the oscillator and most of the internal biasing currents are switched off. Therefore, the functions (tag reader, ISO 9141 driver) are inactive except the voltage regulator and the ISO 9141 receiver on pin K. The driver output TD1 forces a low level and TD2 a high level. A rising edge on K wakes up the circuit. After completion of the wake-up sequence, the circuit is automatically set in read mode.

In configuration A, DOUT and Rx outputs always force a low level, Tx is disabled.

**Figure 6 : Mode access description in one wire bus configuration**



**Figure 7 : Configuration A state diagram**



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## Timing definitions for a 8MHz crystal:

- $T_{ref}$  is crystal oscillator period (125 ns typ.)
- $T_0=8064.T_{ref} = 1.008\text{ms typ.}$
- $T_0'=7932.T_{ref} = 0.992\text{ms typ.}$
- $T_1=16256.T_{ref} = 2.032\text{ms typ.}$
- $T_1'=16128.T_{ref} = 2.016\text{ms typ.}$
- $T_2=4096.T_{ref}, = 512\mu\text{s typ.}$

$T_0$  is the minimum time required to guarantee that the device toggles from read to write (or from write to read). But indeed, the STARC may toggle from read to write (or from write to read) between  $T_0$  and  $T_0'$ .

$T_1$  is the minimum time required to guarantee that the device toggles from write to standby. But indeed, the STARC may toggle in standby between  $T_1$  and  $T_1'$ .

**STANDALONE CONFIGURATION WITH TWO WIRES BUS**

When a low level is applied on MODE1 and a high level on MODE2, the circuit is in **configuration B** (standalone 2 wires bus configuration, see figure 14 page 19).

The K pin is set as an output sending the demodulated data.

The AM pin is set as a VSUP referenced input pin receiving the amplitude modulation and the shutdown/wake-up commands. Forcing high and low levels on AM achieves the amplitude modulation by switching on/off both antenna drivers. Meanwhile, this amplitude modulation can be monitored on the K output. This allows antenna short and open circuit diagnosis.

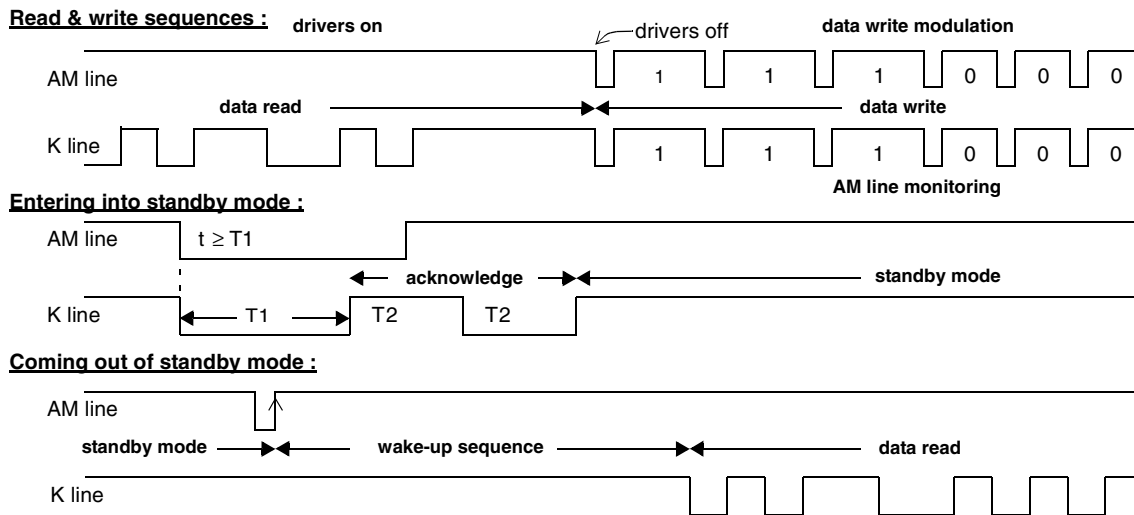
The circuit can be put into **standby mode** by

forcing the AM line at zero during more than 2 ms. The circuit sends an acknowledge pulse before entering into standby mode

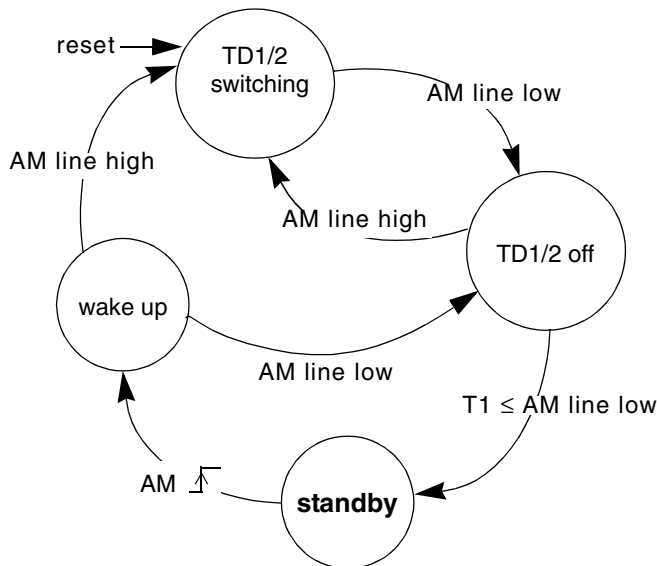
In standby mode, the oscillator and most of the internal biasing currents are switched off. Therefore, the functions (tag reader, ISO 9141 driver) are inactive except the voltage regulator and the ISO 9141 receiver on pin AM. The driver output TD1 forces a low level and TD2 a high level. A rising edge on AM wakes up the circuit. After completion of the wake-up sequence, the circuit is automatically set in read mode.

In configuration B, DOUT and Rx outputs always force a low level, Tx is disabled.

**Figure 8 : Modes access description in two wires bus configuration**



**Figure 9 : Configuration B state diagram**



**DIRECT CONNECTION TO A MICROCONTROLLER CONFIGURATION**

When a high level is applied on MODE1, the circuit is in **configuration C** (direct connection to a microcontroller configuration, see figure 15 page 19).

The demodulated data are sent through DOUT. The AM pin is set as a VDD referenced input pin receiving the AM command. Forcing high and low levels on AM achieves the amplitude modulation by switching on/off both antenna drivers. Meanwhile, this amplitude modulation can be monitored on DOUT. This allows antenna short and open circuit diagnosis.

The circuit can be put into **standby mode** by applying a low level on the MODE2 pin. In standby mode, the oscillator and most of the internal biasing currents are switched off. Therefore, the functions (tag reader, ISO 9141 interface) are inactive except the voltage

regulator. The driver outputs TD1 and TD2 are frozen in their state (high or low level) before entering into standby mode. DOUT forces a low level.

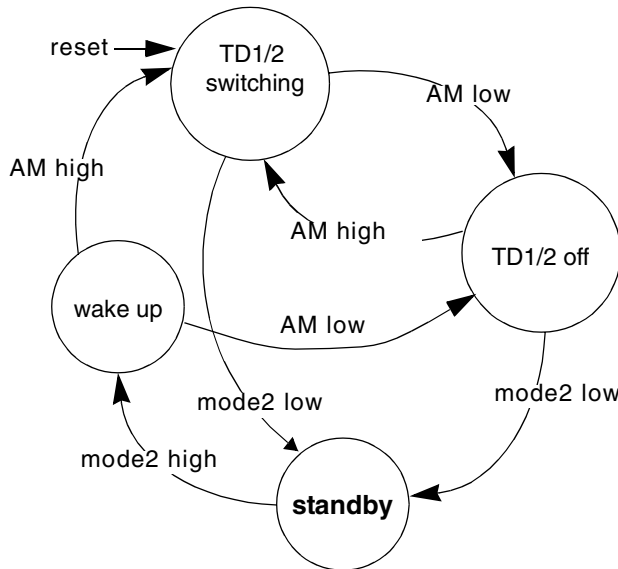
The ISO 9141 interface K is standalone and can be directly controlled by the input pin Tx and monitored by the output Rx.

Applying a logic high level on Tx switches the output driver K on (dominant zero state when an external pull-up resistor is connected between K and VBAT). Applying a logic low level turns the driver off (one recessive state).

Rx monitors the voltage at the K pin. When the voltage is below the low threshold voltage, Rx forces a logic low level. When the voltage is above the high threshold voltage, Rx forces a logic high level.

In standby mode, Tx is disabled and Rx output monitors the voltage at the K pin.

**Figure 10 : Configuration C state diagram**



## ELECTRICAL CHARACTERISTICS

Typical values reflect average measurements at  $V_{SUP}=12V$  and  $T_J=25^{\circ}C$ .

### SUPPLY CURRENT

$6V \leq V_{SUP} \leq 16V$ ,  $V_{SS} = 0V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted

	Parameter	Symbol	Test Conditions & Comments	Min	Typ	Max	Unit	Type
<b>Pin VSUP</b>								
9.1	Standby mode current	$I_{SUP1}$		-	300	500	$\mu A$	
9.2	Operating mode current	$I_{SUP2}$	See note <sup>1</sup>	-	1.5	2.5	mA	

1. Circuit in configuration C, no current sunk from VDD, drivers 1D1/2 switched off, 1x forced to low.

### VOLTAGE REGULATOR

$6V \leq V_{SUP} \leq 16V$ ,  $V_{SS} = 0V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted

	Parameter	Symbol	Test Conditions & Comments	Min	Typ	Max	Unit	Type
<b>Pins VSUP &amp; VDD</b>								
1.1	Output Voltage ( $5.5V \leq V_{SUP} \leq 40V$ )	$V_{VDD1}$	Without external MOS transistor $I_{OUT} \leq 50mA$	4.75	5.0	5.25	V	
1.3	Total Output Current	$I_{VDD1}$		-	-	50	mA	
1.5	Load Regulation	$V_{LoadReg1}$	Without external MOS transistor 1 to 50mA $I_{OUT}$ change	-	20	60	mV	
1.9	Output Voltage ( $5.5V \leq V_{SUP} \leq 40V$ )	$V_{VDD2}$	With external MOS transistor, see notes <sup>1</sup> and <sup>2</sup> $I_{OUT} \leq 150mA$	4.7	5.0	5.3	V	
1.11	Total Output Current	$I_{VDD2}$		-	-	150	mA	
1.6	Load Regulation	$V_{LoadReg2}$	With external MOS transistor 1 to 150mA $I_{OUT}$ change	-	65	150	mV	
1.4	Line Regulation ( $6V \leq V_{SUP} \leq 16V$ )	$V_{LineReg}$	$I_{OUT} = 1mA$	-15	-1	-	mV	

1. The stability is ensured with a decoupling capacitor between VDD and VSS :  $C_{OUT} \geq 10\mu F$  with  $ESR \leq 3\Omega$ .

2. The current capability can be increased up to 150mA by using an external N channel MOS transistor (see figure 1 page 2). The main characteristics for choosing this component are :  $V_T < 1.8V$  and  $BVDSS > 40V$ .

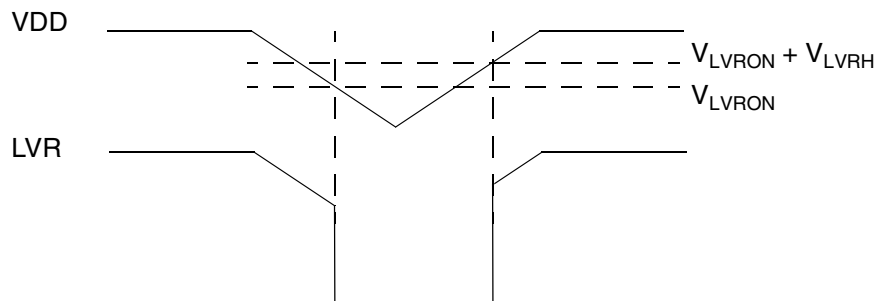
## LOW VOLTAGE RESET

$6V \leq V_{SUP} \leq 16V$ ,  $V_{SS} = 0V$ ,  $T_J = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted

	Parameter	Symbol	Test Conditions & Comments	Min	Typ	Max	Unit	Type
<b>Pin LVR</b>								
1.6	Low Voltage Reset Low Threshold	$V_{LVRON}$	See note <sup>1</sup> and figure 11	4.1	4.35	4.6	V	
1.7	Low Voltage Reset Hysteresis	$V_{LVRH}$		50	100	150	mV	
1.12	Pull-up Current	$I_{LVRUP}$	$V_{LVR} = 2.5V$	5	10	15	$\mu A$	
1.13	Output Resistance in reset condition	$R_{LVR}$	$V_{LVR} = 2.5V$	200	370	500	$\Omega$	
1.14	Input Low Voltage	$V_{ILLVR}$		0	-	$0.3 \times V_{DD}$	V	
1.15	Input High Voltage	$V_{IHLVR}$		$0.7 \times V_{DD}$	-	$V_{DD}$	V	

1. As the voltage regulator and the low voltage reset are using the same internal voltage reference, it is ensured that the low voltage reset will only occur when the voltage regulator is out of regulation.

**Figure 11 : Low voltage reset waveform**



## OSCILLATOR

$6V \leq V_{SUP} \leq 16V$ ,  $V_{SS} = 0V$ ,  $T_J = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted

	Characteristic	Symbol	Test Condition & Comments	Min	Typ	Max	Unit	Type
<b>Pins XTAL1, XTAL2</b>								
8.0	Input Capacitance	$C_{XTAL1}$	$V_{XTAL1} = 2.5V$	-	5	-	pF	
8.1	Voltage gain $V_{XTAL2} / V_{XTAL1}$	$A_{OSC}$	$V_{XTAL1} = 2.5V$	-	25	-	-	
8.3	Clock input level	$V_{XTAL1}$	See note <sup>1</sup>	1.5	-	$V_{DD}$	V <sub>pp</sub>	

1. This level ensures the circuit operation with a 8MHz clock. It is applied through a capacitive coupling. A 1M $\Omega$  resistor connected between XTAL1 and XTAL2 biases the oscillator input.

## TAG READER

$6V \leq V_{SUP} \leq 16V$ ,  $V_{SS} = 0V$ ,  $T_J = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted

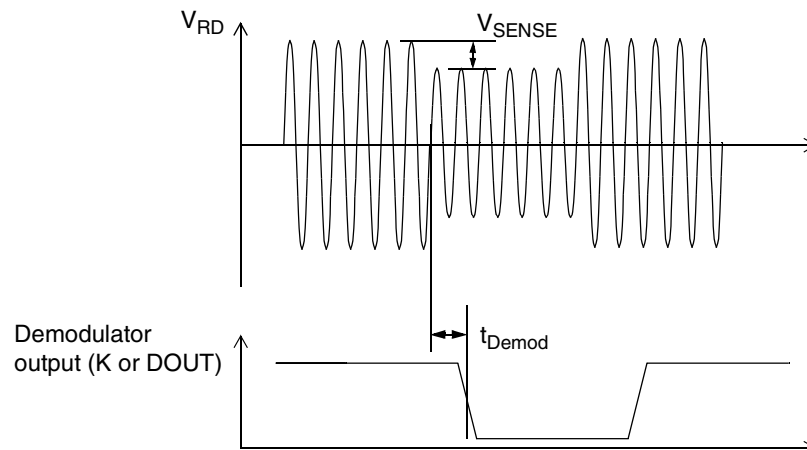
	Parameter	Symbol	Test Conditions & Comments	Min	Typ	Max	Unit	Type
<b>DEMODULATOR (pin RD)</b>								
2.0	Input Voltage Range	$V_{INRD}$		3	4	5	V	
2.2	Input Modulation Frequency	$F_{MOD}$		0.5	4	8	kHz	
2.3	Demodulator Sensitivity	$V_{SENSE1}$	$6.5V \leq V_{SUP} \leq 16V$ See figure 12 and note 1	-	5	15	mV	
2.31	Demodulator Sensitivity	$V_{SENSE2}$	$6V \leq V_{SUP} < 6.5V$ See figure 12 and note 1	-	7	30	mV	
2.4	Demodulation Delay	$t_{Demod}$	See figure 12 Configuration C see note <sup>2</sup> for configurations A and B	-	7.5	10	$\mu s$	
2.5	After Write Pulse Settling Time	$t_{Settling1}$		-	394	400	$\mu s$	
2.6	Recovery Time after wake-up or reset from clock stable to demodulator valid output	$t_{Settling2}$	See note <sup>3</sup>	-	646	700	$\mu s$	
<b>DRIVERS (pins TD1, TD2)</b>								
3.5	Output Carrier Frequency to Crystal Frequency Ratio	$R_{FTD}/F_{XTAL}$		-	64	-	-	
3.0	Turn on/off Delay	$t_{on/off}$		-	-	250	ns	
3.1	Driver1/2 Low Side Out. Resistance	$R_{TDL}$	$I_{LOAD} = 150mA$ DC	-	2.4	4	$\Omega$	
3.2	Driver1/2 High Side Out. Resistance	$R_{TDH}$	$I_{LOAD} = -150mA$ DC	-	2.1	4	$\Omega$	

1. The sensitivity is measured in the following application conditions :  $I_{ANTENNA} = 50mA$  peak,  $V_{RD} = 4V$  peak,  $C_{EXT} = 10nF$ , square wave modulation  $F_{MOD} = F_{TD1}/32$ .

2. Not including the delay due to the slew rate of the K output.

3. Clock stable condition implies  $V_{XTAL1}$  meets the specification (see page 15).

**Figure 12 : Demodulator parameters definition**





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## ISO 9141 INTERFACE

$6V \leq V_{SUP} \leq 16V$ ,  $V_{SS} = 0V$ ,  $T_J = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted

	Parameter	Symbol	Test Conditions & Comments	Min	Typ	Max	Unit	Type
<b>Receiver (pins K &amp; AM)</b>								
4.0	Input Low Voltage	$V_{IL}$		-3	-	$0.3 \times V_{SUP}$	V	
4.1	Input High Voltage	$V_{IH}$		$0.65 \times V_{SUP}$	-	40	V	
4.2	Input Hysteresis Voltage	$V_{HY1}$		0.4	0.65	1.3	V	
4.3	Biassing Current	$I_B$	$0V \leq V_{IN} \leq 16V$	1	3	5	$\mu A$	
4.31	Input Current	$I_{BM}$	$-3 \leq V_{IN} < 0$	-2	-1	-	mA	
4.4	K to Rx delay	tdkrx			2	10	$\mu s$	
<b>Driver (pin K)</b>								
5.0	Output Falling Edge Slew Rate	$SR_F$	$R_{PULL-UP} = 510\Omega$ , see note <sup>1</sup>	3.5	5	6.5	V/ $\mu s$	
5.1	Output Rising Edge Slew Rate	$SR_R$		3.5	5	6.5	V/ $\mu s$	
5.2	Rise Fall Slew Rates Symmetry	$SR_{SYMMETRY}$		-1	0	1	V/ $\mu s$	
5.3	Output Low Voltage	$V_{OLK}$	$I_{LOAD} = 25mA$	-	1.1	1.4	V	
5.4	Input Current (driver switched on or off)	$I_{IK}$	$-3V \leq V_{IN} \leq 0V$	-2	-	0	mA	
5.5	Current Limitation Threshold	$I_L$	$0V \leq V_{IN} \leq 40V$	35	50	65	mA	
5.6	Thermal Shutdown Threshold	$TH_{SDWN}$		130	150	170	$^\circ C$	

1. Calculated from 20% to 80% of the output swing.

## DIGITAL I/O

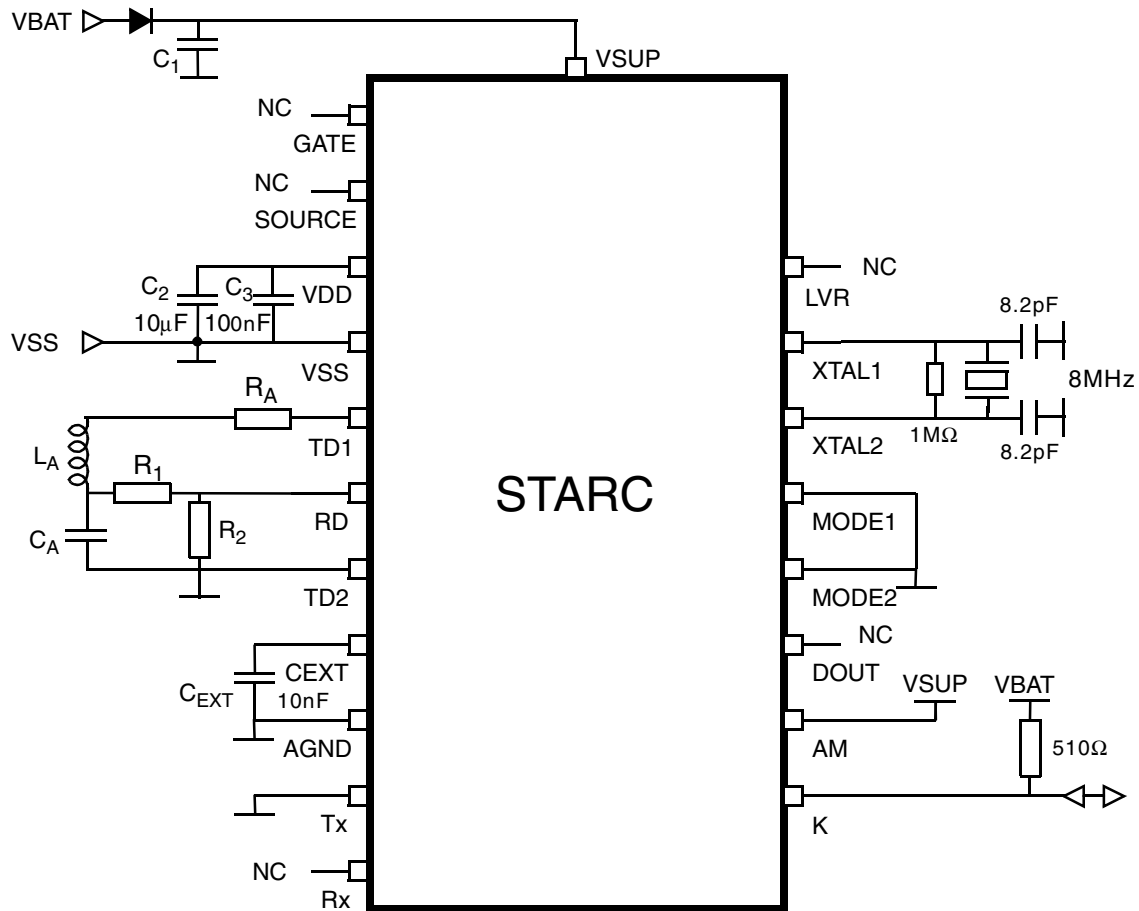
$6V \leq V_{SUP} \leq 16V$ ,  $V_{SS} = 0V$ ,  $T_J = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted

	Characteristic	Symbol	Test Condition & Comments	Min	Typ	Max	Unit	Type
<b>INPUT (pins MODE1, MODE2, AM, TX)</b>								
6.0	Input Low Voltage	$V_{ILD}$		0	-	$0.3 \times V_{DD}$	V	
6.1	Input High Voltage	$V_{IHD}$		$0.7 \times V_{DD}$	-	$V_{DD}$	V	
6.2	Input Hysteresis Voltage	$V_{HD}$		.24	.7	1	V	
<b>OUTPUT (pins DOUT,RX)</b>								
7.0	Output Low Voltage	$V_{OL}$	$I_{LOAD} = 500\mu A$	0	0.5	$0.2 \times V_{DD}$	V	
7.1	Output High Voltage	$V_{OH}$	$I_{LOAD} = -500\mu A$	$0.8 \times V_{DD}$	4.6	$V_{DD}$	V	
7.2	Fall/Rise Time	$t_{F/R}$	$C_{LOAD} = 10pF$ , see note <sup>1</sup>	-	-	150	ns	

1. Calculated from 10% to 90% of the output swing.

APPLICATION SCHEMES

Figure 13 : Standalone configuration with one wire bus



If no external MOS transistor is necessary to increase the voltage regulator current capability, the pins GATE and SOURCE must be left unconnected.

In this configuration, the outputs Rx and DOUT force a low level.

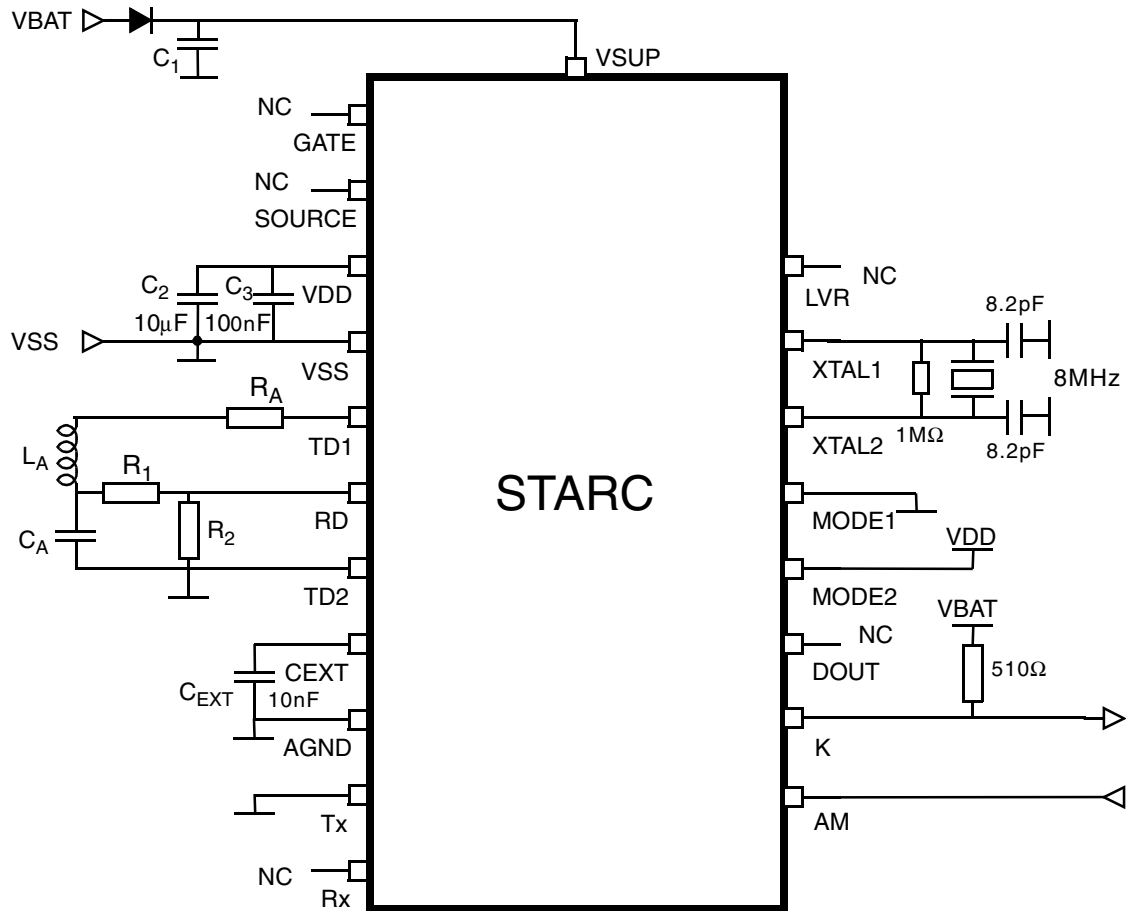
C<sub>1</sub> is not required for the STARC functionality and only acts as a reservoir of energy.

To preserve the demodulator sensitivity, C<sub>EXT</sub> and R<sub>2</sub> should be connected to AGND, and VSS connected to AGND using a low resistance path.

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Figure 14 : Standalone configuration with two wires bus



If no external MOS transistor is necessary to increase the voltage regulator current capability, the pins GATE and SOURCE must be left unconnected.

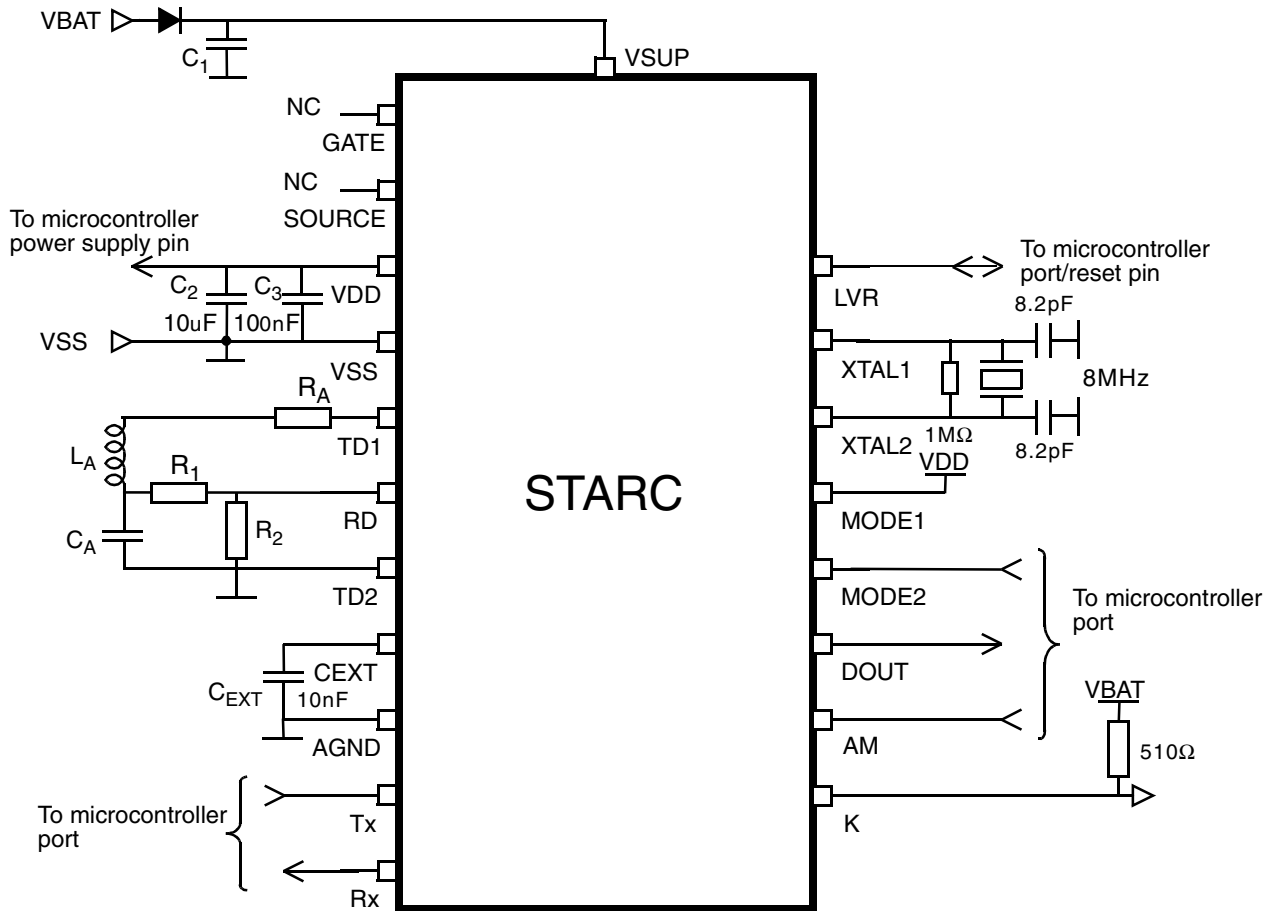
$C_1$  is not required for the STARC functionality and only acts as a reservoir of energy.

To preserve the demodulator sensitivity,  $C_{EXT}$  and  $R_2$  should be connected to AGND, and VSS connected to AGND using a low resistance path.

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Figure 15 : Direct connection to a microcontroller



If no external MOS transistor is necessary to increase the voltage regulator current capability, the pins GATE and SOURCE must be left unconnected.

C<sub>1</sub> is not required for the STARC functionality and only acts as a reservoir of energy.

To preserve the demodulator sensitivity, C<sub>EXT</sub> and R<sub>2</sub> should be connected to AGND, and VSS connected to AGND using a low resistance path.

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